WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Thursday, September 15, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; PLUR=YES; OP=ADJ	
☐	L6	L5 and $epitaxial$	20
☐	L5	L4 and processing	50
☐	L4	L2 and clean$	71
☐	L3	L2 with clean$	0
☐	L2	(integrated circuit) with ($doped polysilicon)	484
☐	L1	(integrated circuit) and ($doped polysilicon)	10241

END OF SEARCH HISTORY

WEST Search History

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DATE: Thursday, September 15, 2005

Hide?	Set Name	Query	Hit Count
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
☐	L16	L15 with (NF3 or (nitrogen adj fluoride))	2
☐	L15	L14 with (hf or (hydrogen fluoride))	694
☐	L14	L13 with (semiconductor or wafer or (integrated adj circuit))	73554
☐	L13	(remov$ or decontaminat$ or clean$)	2083075
	DB=PGPB,USPT; PLUR=YES; OP=ADJ		
☐	L12	L8 and forming and layers	21
☐	L11	L8 and (hydrogen bake)	1
☐	L10	L8 and (polysilicon deposition)	1
☐	L9	L8 and (polysilicon adj deposition)	1
☐	L8	L4 and (134/2 or 134/3 or 134/19 or 134/26 or 134/28 or 134/41 or 134/902 or 134/25.4).ccls.	26
☐	L7	L4 and (nitrogen containing gas)	3
☐	L6	L4 and (NF3 or (nitrogen adj fluoride))	1
☐	L5	L4 with (NF3 or (nitrogen adj fluoride))	0
☐	L4	L3 with RCA	109
☐	L3	L2 with (hf or (hydrogen fluoride))	2886
☐	L2	L1 with (semiconductor or wafer or (integrated adj circuit))	103794
☐	L1	(remov$ or decontaminat$ or clean$)	2585065

END OF SEARCH HISTORY

Hit List

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: JP 07263416 A

Using default format because multiple data bases are involved.

L16: Entry 1 of 2 File: JPAB Oct 13, 1995

PUB-NO: JP407263416A
DOCUMENT-IDENTIFIER: JP 07263416 A
TITLE: METHOD AND DEVICE OF MANUFACTURING SEMICONDUCTOR DEVICE

PUBN-DATE: October 13, 1995

INVENTOR-INFORMATION:

NAME	COUNTRY
KIKUCHI, JUN	

INT-CL (IPC): H01 L 21/3065; H01 L 21/306

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 2. Document ID: US 20040074285 A1, WO 2004036175 A2, AU 2003301333 A1, EP 1554561 A2

L16: Entry 2 of 2 File: DWPI Apr 22, 2004

DERWENT-ACC-NO: 2004-398326
DERWENT-WEEK: 200547
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Gas sensor assembly for detecting fluorine-containing species in, e.g. semiconductor processing tool effluent, includes free-standing gas sensing element formed of material exhibiting change in contact with fluoro species

INVENTOR: BAUM, T H; CHEN, P S ; CHEN, S ; DIMEO, F ; KING, M E ; NEUNER, J W ; ROEDER, J F ; STAWASZ, M ; WELCH, J ; CHEN, I ; CHEN, P S H ; CHEN, -

PRIORITY-DATA: 2002US-0273036 (October 17, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20040074285 A1	April 22, 2004		038	G01N027/04
WO 2004036175 A2	April 29, 2004	E	000	G01N000/00
AU 2003301333 A1	May 4, 2004		000	G01N027/04
EP 1554561 A2	July 20, 2005	E	000	G01N009/00

INT-CL (IPC): G01 N 0/00; G01 N 9/00; G01 N 27/04; H01 L 21/66

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
NF3	954
NF3S	0
NITROGEN	207145
NITROGENS	439
FLUORIDE	61610
FLUORIDES	4442
(15 WITH (NF3 OR (NITROGEN ADJ FLUORIDE))).EPAB,JPAB,DWPI,TDBD.	2
(L15 WITH (NF3 OR (NITROGEN ADJ FLUORIDE))).EPAB,JPAB,DWPI,TDBD.	2

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Hit List

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: JP 07263416 A

Using default format because multiple data bases are involved.

L16: Entry 1 of 2 File: JPAB Oct 13, 1995

PUB-NO: JP407263416A
DOCUMENT-IDENTIFIER: JP 07263416 A
TITLE: METHOD AND DEVICE OF MANUFACTURING SEMICONDUCTOR DEVICE

PUBN-DATE: October 13, 1995

INVENTOR-INFORMATION:

NAME	COUNTRY
KIKUCHI, JUN	

INT-CL (IPC): H01 L 21/3065; H01 L 21/306

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

☐ 2. Document ID: US 20040074285 A1, WO 2004036175 A2, AU 2003301333 A1, EP 1554561 A2

L16: Entry 2 of 2 File: DWPI Apr 22, 2004

DERWENT-ACC-NO: 2004-398326
DERWENT-WEEK: 200547
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Gas sensor assembly for detecting fluorine-containing species in, e.g. semiconductor processing tool effluent, includes free-standing gas sensing element formed of material exhibiting change in contact with fluoro species

INVENTOR: BAUM, T H; CHEN, P S ; CHEN, S ; DIMEO, F ; KING, M E ; NEUNER, J W ; ROEDER, J F ; STAWASZ, M ; WELCH, J ; CHEN, I ; CHEN, P S H ; CHEN, -

PRIORITY-DATA: 2002US-0273036 (October 17, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20040074285 A1	April 22, 2004		038	G01N027/04
WO 2004036175 A2	April 29, 2004	E	000	G01N000/00
AU 2003301333 A1	May 4, 2004		000	G01N027/04
EP 1554561 A2	July 20, 2005	E	000	G01N009/00

INT-CL (IPC): G01 N 0/00; G01 N 9/00; G01 N 27/04; H01 L 21/66

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
NF3	954
NF3S	0
NITROGEN	207145
NITROGENS	439
FLUORIDE	61610
FLUORIDES	4442
(15 WITH (NF3 OR (NITROGEN ADJ FLUORIDE))).EPAB,JPAB,DWPI,TDBD.	2
(L15 WITH (NF3 OR (NITROGEN ADJ FLUORIDE))).EPAB,JPAB,DWPI,TDBD.	2

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L16: Entry 1 of 2 File: JPAB Oct 13, 1995

DOCUMENT-IDENTIFIER: JP 07263416 A
TITLE: METHOD AND DEVICE OF MANUFACTURING SEMICONDUCTOR DEVICE

Abstract Text (1):
PURPOSE: To enable a natural oxide film on a semiconductor substrate surface to be efficiently removed by a method wherein a substrate treated with HF vapor and H20 or alcohol vapor in the nitrogen fluoride containing gas added down stream gas is to be treated by exposing in hydrogen containing plasmatic gas.

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L16: Entry 1 of 2 File: JPAB Oct 13, 1995

PUB-NO: JP407263416A
DOCUMENT-IDENTIFIER: JP 07263416 A
TITLE: METHOD AND DEVICE OF MANUFACTURING SEMICONDUCTOR DEVICE

PUBN-DATE: October 13, 1995

INVENTOR-INFORMATION:
NAME COUNTRY
KIKUCHI, JUN

ASSIGNEE-INFORMATION:
NAME COUNTRY
FUJITSU LTD

APPL-NO: JP06049547
APPL-DATE: March 18, 1994

INT-CL (IPC): H01 L 21/3065; H01 L 21/306

ABSTRACT:

PURPOSE: To enable a natural oxide film on a semiconductor substrate surface to be efficiently removed by a method wherein a substrate treated with HF vapor and H20 or alcohol vapor in the nitrogen fluoride containing gas added down stream gas is to be treated by exposing in hydrogen containing plasmatic gas.

CONSTITUTION: A Teflon made jig 106 is arranged in a Teflon made airtight vessel 105 so as to mount a silicon wafer 104 on the jig 106. On the other hand, a mixed gas of HF, H20, N2 is fed downward from the vessel 105 to be exhausted from the lower exhaust port. Through these procedures, the natural oxide film on the wafer 104 can be easily removed by feeding HF vapor properly mixed with other gasses. Next, the silicon wafer 104 with the natural oxide film removed by the HF vapor is mounted on a susceptor 112 in a down flow treating chamber 110. Through this down flow Wing step, the residual reaction products on the wafer 104 surface can be efficiently removed.

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Hit List

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Search Results - Record(s) 11 through 20 of 21 returned.

☐ 11. Document ID: US 6656289 B2

Using default format because multiple data bases are involved.

L12: Entry 11 of 21 File: USPT Dec 2, 2003

US-PAT-NO: 6656289
DOCUMENT-IDENTIFIER: US 6656289 B2

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

DATE-ISSUED: December 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 134/3; 134/2, 134/28, 134/30, 134/902, 257/E21.228

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 12. Document ID: US 6645311 B2

L12: Entry 12 of 21 File: USPT Nov 11, 2003

US-PAT-NO: 6645311
DOCUMENT-IDENTIFIER: US 6645311 B2

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 134/28; 134/2, 134/30, 134/31, 134/902, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel.

16 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 13. Document ID: US 6641677 B1

L12: Entry 13 of 21 File: USPT Nov 4, 2003

US-PAT-NO: 6641677
DOCUMENT-IDENTIFIER: US 6641677 B1
**** See image for Certificate of Correction ****

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

DATE-ISSUED: November 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 134/28; 134/3, 134/30, 134/902, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel. In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Following the chemical treatment, the semiconductor structure is transferred directly to a second treatment vessel where it is rinsed with DI water and then dried. The second treatment vessel is flooded with both DI water and a gas that is inert to the ambient, such as nitrogen, to form a DI water bath upon which an inert atmosphere is maintained during rinsing. Next, an inert gas carrier laden with IPA vapor is fed into the second treatment vessel. After sufficient time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. The semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, to be entrained beneath the IPA-DI water interface. In a second embodiment of the present invention, chemical treatment, rinsing, and drying are carried out in a single vessel. In a third embodiment of the present invention, a retrofit spray/dump rinser with a lid is used for rinsing and drying according to the method of the present invention.

34 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 14. Document ID: US 6607001 B1

L12: Entry 14 of 21 File: USPT Aug 19, 2003

US-PAT-NO: 6607001
DOCUMENT-IDENTIFIER: US 6607001 B1
**** See image for Certificate of Correction ****

TITLE: System of reducing water spotting and oxide growth on a semiconductor structure

DATE-ISSUED: August 19, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 134/95.2; 134/102.1, 134/186, 134/902, 134/99.1, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel.

22 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 15. Document ID: US 6601595 B2

L12: Entry 15 of 21 File: USPT Aug 5, 2003

US-PAT-NO: 6601595
DOCUMENT-IDENTIFIER: US 6601595 B2
**** See image for Certificate of Correction ****

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

DATE-ISSUED: August 5, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 134/95.2; 134/102.1, 134/186, 134/902, 134/99.1, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor

structure in a modified conventional gas etch/rinse or dryer vessel.

19 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

☐ 16. Document ID: US 6350322 B1

L12: Entry 16 of 21 File: USPT Feb 26, 2002

US-PAT-NO: 6350322
DOCUMENT-IDENTIFIER: US 6350322 B1
**** See image for Certificate of Correction ****

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

DATE-ISSUED: February 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 134/3; 134/11, 134/2, 134/26, 134/28, 134/30, 134/31, 134/902, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel. In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Following the chemical treatment, the semiconductor structure is transferred directly to a second treatment vessel where it is rinsed with DI water and then dried. The second treatment vessel is flooded with both DI water and a gas that is inert to the ambient, such as nitrogen, to form a DI water bath upon which an inert atmosphere is maintained during rinsing. Next, an inert gas carrier laden with IPA vapor is fed into the second treatment vessel. After sufficient time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. The semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, to be entrained beneath the IPA-DI water interface. In a second embodiment of the present invention, chemical treatment, rinsing, and drying are carried out in a single vessel. In a third embodiment of the present invention, a retrofit spray/dump rinser with a lid is used for rinsing and drying according to the method of the present invention.

26 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

☐ 17. Document ID: US 6336463 B1

L12: Entry 17 of 21 File: USPT Jan 8, 2002

US-PAT-NO: 6336463
DOCUMENT-IDENTIFIER: US 6336463 B1

TITLE: Cleaning/drying station and production line for semiconductor devices

DATE-ISSUED: January 8, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ohta; Nahomi	Tokyo			JP

US-CL-CURRENT: 134/61; 134/102.3, 134/902, 134/95.2

ABSTRACT:

A production line includes a centralized cleaning/drying station for cleaning a wafer by using an HF cleaning solution or a non-HF cleaning solution and subsequently drying the wafer based on the desired cleaning/drying conditions, and a transport system for transporting the wafer between each processing station and the centralized cleaning/drying station. The production line has a large flexibility for selecting the cleaning/drying conditions for the wafer with a reduced system size.

8 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

☐ 18. Document ID: US 6319331 B1

L12: Entry 18 of 21 File: USPT Nov 20, 2001

US-PAT-NO: 6319331
DOCUMENT-IDENTIFIER: US 6319331 B1

TITLE: Method for processing semiconductor substrate

DATE-ISSUED: November 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kume; Morihiko	Tokyo			JP
Yamamoto; Hidekazu	Tokyo			JP

US-CL-CURRENT: 134/3; 134/2, 134/21, 257/E21.228, 257/E21.285

ABSTRACT:

An object is to provide a method for processing a semiconductor substrate that can form an oxide film less prone to take in impurities affecting semiconductor characteristics on the surface. An RCA-cleaned semiconductor substrate is treated with diluted hydrofluoric acid (HF) to remove a native oxide film formed on the semiconductor substrate during the RCA cleaning process (step S8). For conditions of the treatment with diluted hydrofluoric acid, the concentration of hydrofluoric acid is about 50%, the ratio of hydrofluoric acid to pure water is 1:100, and the processing time is about one minute. Finally, the semiconductor substrate from which the native oxide film has been removed is stored in a clean atmosphere of oxygen for a predetermined time period to form an oxide film on the semiconductor substrate surface (step S9). The percentage of oxygen in the atmosphere of oxygen in the place for storage is about 20 to 100%.

7 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

☐ 19. Document ID: US 5845660 A

L12: Entry 19 of 21 File: USPT Dec 8, 1998

US-PAT-NO: 5845660
DOCUMENT-IDENTIFIER: US 5845660 A

TITLE: Substrate washing and drying apparatus, substrate washing method, and substrate washing apparatus

DATE-ISSUED: December 8, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shindo; Naoki	Nirasaki			JP
Kamikawa; Yuuji	Kumamoto-ken			JP
Mokuo; Shori	Saga-ken			JP
Kumagai; Yoshio	Yamanashi-ken			JP

US-CL-CURRENT: 134/56R; 134/102.3, 134/113, 134/186, 134/902, 134/95.3

ABSTRACT:

A substrate washing and drying apparatus comprising a processing section for holding wafers, to which process solution to wash and vapor for drying the wafers are introduced, a supply/discharge port for introducing solution to the process section, and discharging the solution from the process section, a solution supply mechanism for selecting one from a plurality of kinds of solution, a drying vapor generation section having a heater for generation vapor for drying, a discharging solution mechanism having an opening for rapidly discharging the solution from the

processing section, resistivity detecting means for detecting a resistivity value of the process solution, and a controller for controlling the supply of solution to the process section based on the resistivity value detected by the resistivity detecting means.

20 Claims, 21 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 16

☐ 20. Document ID: US 5350480 A

L12: Entry 20 of 21 File: USPT Sep 27, 1994

US-PAT-NO: 5350480
DOCUMENT-IDENTIFIER: US 5350480 A
**** See image for Certificate of Correction ****

TITLE: Surface cleaning and conditioning using hot neutral gas beam array

DATE-ISSUED: September 27, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gray; David C.	Sunnyvale	CA		

US-CL-CURRENT: 156/345.26; 134/31, 134/902, 156/345.27, 156/345.37, 216/58, 216/59, 257/E21.226

ABSTRACT:

An apparatus for generating large arrays of directed beams containing thermally excited, electrically neutral gas species, including vibrationally excited molecules, free radicals, and atoms, is disclosed. A heated plate in which a designed array of long, narrow channels are formed serves both to activate and collimate the gas species, and separates a high pressure reservoir of reactive gas from an evacuated region which serves as the material processing chamber. Selection of the appropriate reservoir pressure and channel geometry facilitates the thermal excitation of the reactive gas through collisions with hot channel walls, and the formation of directed non-collisional beams which may be readily transported through the evacuated chamber. The heated channel array plate is designed to allow good gas flux uniformity over a large target area by appropriately setting the pitch spacing and aspect ratio of the channels. Impingement of the thermally excited neutral gas species on a target material allows cleaning of surface contaminations and residues, removal of material surface layers without causing ballistic damage, or reactive modification of the surface layers. The directionality or angular divergence of the beams may be tuned to adjust the anisotropy of the surface cleaning and/or etching, allowing transport of thermally excited species into high aspect ratio target surface structures.

23 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 9

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Term	Documents
FORMING	1909476
FORMINGS	289
LAYERS	741877
LAYER	1220716
(8 AND FORMING AND LAYERS).PGPB,USPT.	21
(L8 AND FORMING AND LAYERS).PGPB,USPT.	21

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Search Results - Record(s) 21 through 21 of 21 returned.

☐ 21. Document ID: US 4752505 A

Using default format because multiple data bases are involved.

L12: Entry 21 of 21 File: USPT Jun 21, 1988

US-PAT-NO: 4752505
DOCUMENT-IDENTIFIER: US 4752505 A

TITLE: Pre-metal deposition cleaning for bipolar semiconductors

DATE-ISSUED: June 21, 1988

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Arac; Sabri	Concord	CA		

US-CL-CURRENT: 438/750; 134/1.3, 134/3, 134/41, 257/E21.162, 257/E21.251, 427/307, 427/318, 438/597, 438/756, 438/974

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
FORMING	1909476
FORMINGS	289
LAYERS	741877
LAYER	1220716
(8 AND FORMING AND LAYERS).PGPB,USPT.	21
(L8 AND FORMING AND LAYERS).PGPB,USPT.	21

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Search Results - Record(s) 1 through 10 of 21 returned.

☐ 1. Document ID: US 20050133068 A1

Using default format because multiple data bases are involved.

L12: Entry 1 of 21 File: PGPB Jun 23, 2005

PGPUB-DOCUMENT-NUMBER: 20050133068
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050133068 A1

TITLE: Method for cleaning a creamic member for use in a system for producing semiconductors, a cleaning agent and a combination of cleaning agents

PUBLICATION-DATE: June 23, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yamaguchi, Shinji	Ama-gun		JP	
Kiku, Taiji	Handa-city		JP	
Kondou, Nobuyuki	Handa-city		JP	

US-CL-CURRENT: 134/26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

☐ 2. Document ID: US 20050089489 A1

L12: Entry 2 of 21 File: PGPB Apr 28, 2005

PGPUB-DOCUMENT-NUMBER: 20050089489
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050089489 A1

TITLE: Composition for exfoliation agent effective in removing resist residues

PUBLICATION-DATE: April 28, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Carter, Melvin K.	Los Gatos	CA	US	

US-CL-CURRENT: 424/70.1; 134/2, 134/26

ABSTRACT:

Improved fluoride-based compositions effective in exfoliating resist residues resulting from dry etching and plasma ashing are disclosed. An excellent anti-corrosion effect, as well as resist residue exfoliation effect, can be achieved using the disclosed compositions.

☐ 3. Document ID: US 20040139991 A1

L12: Entry 3 of 21 File: PGPB Jul 22, 2004

PGPUB-DOCUMENT-NUMBER: 20040139991
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040139991 A1

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

PUBLICATION-DATE: July 22, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yates, Donald L.	Boise	ID	US	

US-CL-CURRENT: 134/28; 134/26, 134/3, 134/30, 134/31, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel.

☐ 4. Document ID: US 20040123882 A1

L12: Entry 4 of 21 File: PGPB Jul 1, 2004

PGPUB-DOCUMENT-NUMBER: 20040123882
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040123882 A1

TITLE: In-situ removal of surface impurities prior to arsenic-doped polysilicon deposition in the fabrication of a heterojunction bipolar transistor

PUBLICATION-DATE: July 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47

Olmer, Leonard J.	Orlando	FL	US
Jones, Robert F.	Clermont	FL	US
Bevers, William D.	Orlando	FL	US
Martin, Edward P. JR.	Orlando	FL	US

US-CL-CURRENT: 134/28; 134/2, 134/26, 134/3, 134/37, 427/523

ABSTRACT:

A process for cleaning the silicon surface of a semiconductor device material layer. The surface undergoes a pre-clean process followed by exposure to a nitrogen-containing gas. A polysilicon layer is formed on the surface in the same chamber and at about the same temperature as the cleaning and nitrogen exposing steps.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 20030192574 A1

L12: Entry 5 of 21 File: PGPB Oct 16, 2003

PGPUB-DOCUMENT-NUMBER: 20030192574
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030192574 A1

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

PUBLICATION-DATE: October 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yates, Donald L.	Boise	ID	US	

US-CL-CURRENT: 134/28; 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 20030000554 A1

L12: Entry 6 of 21 File: PGPB Jan 2, 2003

PGPUB-DOCUMENT-NUMBER: 20030000554
PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030000554 A1

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

PUBLICATION-DATE: January 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yates, Donald L.	Boise	ID	US	

US-CL-CURRENT: 134/95.2; 134/902, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel. In an embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Following the chemical treatment, the semiconductor structure is transferred directly to a second treatment vessel where it is rinsed with DI water and then dried. The second treatment vessel is flooded with both DI water and a gas that is inert to the ambient, such as nitrogen, to form a DI water bath upon which an inert atmosphere is maintained during rinsing. Next, an inert gas carrier laden with IPA vapor is fed into the second treatment vessel. After sufficient time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. The semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, to be entrained beneath the IPA-DI water interface. In a second embodiment of the present invention, chemical treatment, rinsing, and drying are carried out in a single vessel. In a third embodiment of the present invention, a retrofit spray/dump rinser with a lid is used for rinsing and drying according to the method of the present invention.

☐ 7. Document ID: US 20020023669 A1

L12: Entry 7 of 21 File: PGPB Feb 28, 2002

PGPUB-DOCUMENT-NUMBER: 20020023669
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020023669 A1

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

PUBLICATION-DATE: February 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yates, Donald L.	Boise	ID	US	

US-CL-CURRENT: 134/30; 134/2, 134/21, 134/26, 134/28, 134/3, 134/31, 134/34,

134/37, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel. In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Following the chemical treatment, the semiconductor structure is transferred directly to a second treatment vessel where it is rinsed with DI water and then dried. The second treatment vessel is flooded with both DI water and a gas that is inert to the ambient, such as nitrogen, to form a DI water bath upon which an inert atmosphere is maintained during rinsing. Next, an inert gas carrier laden with IPA vapor is fed into the second treatment vessel. After sufficient time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. The semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, to be entrained beneath the IPA-DI water interface. In a second embodiment of the present invention, chemical treatment, rinsing, and drying are carried out in a single vessel. In a third embodiment of the present invention, a retrofitted spray/dump rinser with a lid is used for rinsing and drying according to the method of the present invention.

☐ 8. Document ID: US 20010015212 A1

L12: Entry 8 of 21 File: PGPB Aug 23, 2001

PGPUB-DOCUMENT-NUMBER: 20010015212
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010015212 A1

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

PUBLICATION-DATE: August 23, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yates, Donald L.	Boise	ID	US	

US-CL-CURRENT: 134/2; 134/26, 134/27, 134/3, 134/30, 134/31, 134/32, 134/34, 134/37, 134/902, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel. In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Following the chemical treatment, the semiconductor structure is transferred directly to a second treatment vessel where it is rinsed with DI water and then dried. The second treatment vessel is flooded with both DI water and a gas that is inert to the ambient, such as nitrogen, to form a DI water bath upon which an inert atmosphere is maintained

during rinsing. Next, an inert gas carrier laden with IPA vapor is fed into the second treatment vessel. After sufficient time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. The semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, to be entrained beneath the IPA-DI water interface. In a second embodiment of the present invention, chemical treatment, rinsing, and drying are carried out in a single vessel. In a third embodiment of the present invention, a retrofit spray/dump rinser with a lid is used for rinsing and drying according to the method of the present invention.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 9. Document ID: US 6896740 B2

L12: Entry 9 of 21 File: USPT May 24, 2005

US-PAT-NO: 6896740
DOCUMENT-IDENTIFIER: US 6896740 B2

TITLE: Method of reducing water spotting and oxide growth on a semiconductor structure

DATE-ISSUED: May 24, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 134/3; 134/11, 134/2, 134/26, 134/28, 134/30, 134/31, 134/902, 257/E21.228

ABSTRACT:

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer vessel. In an embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Following the chemical treatment, the semiconductor structure is transferred directly to a second treatment vessel where it is rinsed with DI water and then dried. The second treatment vessel is flooded with both DI water and a gas that is inert to the ambient, such as nitrogen, to form a DI water bath upon which an inert atmosphere is maintained during rinsing. Next, an inert gas carrier laden with IPA vapor is fed into the second treatment vessel. After sufficient time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. The semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, to be entrained beneath the IPA-DI water interface.

25 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

☐ 10. Document ID: US 6884721 B2

L12: Entry 10 of 21 File: USPT Apr 26, 2005

US-PAT-NO: 6884721
DOCUMENT-IDENTIFIER: US 6884721 B2

TITLE: Silicon wafer storage water and silicon wafer storage method

DATE-ISSUED: April 26, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fukami; Teruaki	Fukushima-ken			JP

US-CL-CURRENT: 438/690; 134/2, 257/E21.228, 438/692

ABSTRACT:

Storage water used for storage of a silicon wafer in water is disclosed. The storage water contains Cu at a concentration of 0.01 ppb or less. A method of storing a silicon wafer in water is also disclosed. In the method, water containing Cu at a concentration of 0.01 ppb or less is used. In another method, a wafer is stored in water or a chemical solution, to which a chelating agent is added. The storage water and the storage methods can prevent degradation of oxide dielectric breakdown voltage which would otherwise occur due to Cu contamination from the storage water.

6 Claims, 1 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

Term	Documents
FORMING	1909476
FORMINGS	289
LAYERS	741877
LAYER	1220716
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(L8 AND FORMING AND LAYERS).PGPB,USPT.	21

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☐ 1. Document ID: US 20040125538 A1

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L6: Entry 1 of 20 File: PGPB Jul 1, 2004

PGPUB-DOCUMENT-NUMBER: 20040125538
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040125538 A1

TITLE: Method for improved processing and etchback of a container capacitor

PUBLICATION-DATE: July 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Carstensen, Robert K.	Boise	ID	US	

US-CL-CURRENT: 361/305; 257/E21.019, 257/E21.648

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20040110345 A1

L6: Entry 2 of 20 File: PGPB Jun 10, 2004

PGPUB-DOCUMENT-NUMBER: 20040110345
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040110345 A1

TITLE: Vertical replacement-gate junction field-effect transistor

PUBLICATION-DATE: June 10, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chaudhry, Samir	Orlando	FL	US	
Layman, Paul Arthur	Orlando	FL	US	
McMacken, John Russell	Orlando	FL	US	
Thomson, Ross	Clermont	FL	US	
Zhao, Jack Qingsheng	Orefield	PA	US	

US-CL-CURRENT: 438/270; 257/134, 257/272, 257/E21.447, 257/E21.629, 257/E27.06,

257/E27.069, 257/E29.313, 438/191, 438/192, 438/268

ABSTRACT:

An architecture for creating a vertical JFET. Generally, an integrated circuit structure includes a semiconductor area with a major surface formed along a plane and a first source/drain doped region formed in the surface. A second doped region forming a channel of different conductivity type than the first region is positioned over the first region. A third doped region is formed over the second doped region having an opposite conductivity type with respect to the second doped region, and forming a source/drain region. A gate is formed over the channel to form a vertical JFET.

In an associated method of manufacturing the semiconductor device, a first source/drain region is formed in a semiconductor layer. A field-effect transistor gate region, including a channel and a gate electrode, is formed over the first source/drain region. A second source/drain region is then formed over the channel having the appropriate conductivity type.

☐ 3. Document ID: US 20030047749 A1

L6: Entry 3 of 20 File: PGPB Mar 13, 2003

PGPUB-DOCUMENT-NUMBER: 20030047749
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030047749 A1

TITLE: Vertical replacement-gate junction field-effect transistor

PUBLICATION-DATE: March 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chaudhry, Samir	Orlando	FL	US	
Layman, Paul Arthur	Orlando	FL	US	
McMacken, John Russell	Orlando	FL	US	
Thomson, Ross	Clermont	FL	US	
Zhao, Jack Qingsheng	Orefield	PA	US	

US-CL-CURRENT: 257/135; 257/134, 257/263, 257/272, 257/E21.447, 257/E21.629, 257/E27.06, 257/E27.069, 257/E29.313, 438/268, 438/270

ABSTRACT:

An architecture for creating a vertical JFET. Generally, an integrated circuit structure includes a semiconductor area with a major surface formed along a plane and a first source/drain doped region formed in the surface. A second doped region forming a channel of different conductivity type than the first region is positioned over the first region. A third doped region is formed over the second doped region having an opposite conductivity type with respect to the second doped region, and forming a source/drain region. A gate is formed over the channel to

form a vertical JFET.

In an associated method of manufacturing the semiconductor device, a first source/drain region is formed in a semiconductor layer. A field-effect transistor gate region, including a channel and a gate electrode, is formed over the first source/drain region. A second source/drain region is then formed over the channel having the appropriate conductivity type.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 20020000596 A1

L6: Entry 4 of 20 File: PGPB Jan 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020000596
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020000596 A1

TITLE: Method for improved processing and etchback of a container capacitor

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Carstensen, Robert K.	Boise	ID	US	

US-CL-CURRENT: 257/296; 257/300, 257/301, 257/303, 257/E21.019, 257/E21.648

ABSTRACT:

A capacitor having improved size for enhanced capacitance and a method of forming the same are disclosed. In one embodiment, the capacitor is a stacked container capacitor used in a dynamic random access memory circuit. The capacitor provides a capacitor that has high storage capacitance which provides an increased efficiency for a cell without an increase in the size of the cell.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 20010024853 A1

L6: Entry 5 of 20 File: PGPB Sep 27, 2001

PGPUB-DOCUMENT-NUMBER: 20010024853
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010024853 A1

TITLE: High charge storage density integrated circuit capacitor

PUBLICATION-DATE: September 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wallace, Robert M.	Richardson	TX	US	
Wilk, Glen D.	New Providence	NJ	US	
Anthony, Mark	Tampa	FL	US	
Kwong, Dim-Lee	Austin	TX	US	

US-CL-CURRENT: 438/240; 257/E21.193, 257/E21.272, 257/E29.162

ABSTRACT:

An integrated circuit capacitor comprising a high permittivity dielectric and a method of forming the same are disclosed herein. In one embodiment, this capacitor may be used as a DRAM storage cell. For example, a DRAM storage node electrode 22 may be formed of polysilicon. An ultrathin oxynitride passivation layer 25 (e.g. less than 1 nm) is formed on this electrode by exposure of the substrate to NO. A tantalum pentoxide layer 24 is formed over layer 25, followed by a cell plate 26. Passivation layer 25 allows electrode 22 to resist oxidation during deposition of layer 25, thus preventing formation of an interfacial oxide layer. A passivation layer formed by this method may typically be deposited with shorter exposure times and lower temperatures than nitride passivation layers.

☐ 6. Document ID: US 6833084 B2

L6: Entry 6 of 20 File: USPT Dec 21, 2004

US-PAT-NO: 6833084
DOCUMENT-IDENTIFIER: US 6833084 B2

TITLE: Etching compositions

DATE-ISSUED: December 21, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mercaldi; Garry A.	Meridian	ID		
Yates; Donald L.	Boise	ID		

US-CL-CURRENT: 252/79.1; 252/79.2, 252/79.3, 252/79.4, 257/E21.309, 438/745, 438/753

ABSTRACT:

The present invention provides an etching composition which includes a polyhydric alcohol in combination with two inorganic acids. Preferably the etching composition of the present invention is a mixture of a glycol, nitric acid and hydrofluoric acid, with propylene glycol being preferred. The etching composition of the present invention achieves a selectivity of greater than 70:1, doped material to undoped material. The present invention provides an etching formulation which has increased selectivity of doped polysilicon to undoped polysilicon and provides an efficient

integrated circuit fabrication process without requiring time consuming and costly processing modifications to the etching apparatus or production apparatus.

28 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

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☐ 7. Document ID: US 6693015 B2

L6: Entry 7 of 20 File: USPT Feb 17, 2004

US-PAT-NO: 6693015
DOCUMENT-IDENTIFIER: US 6693015 B2
**** See image for Certificate of Correction ****

TITLE: Method for improved processing and etchback of a container capacitor

DATE-ISSUED: February 17, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Carstensen; Robert K.	Boise	ID		

US-CL-CURRENT: 438/306; 257/E21.019, 257/E21.648, 438/239, 438/242, 438/253, 438/296, 438/301, 438/303, 438/310, 438/387 , 438/396, 438/532

ABSTRACT:

A capacitor having improved size for enhanced capacitance and a method of forming the same are disclosed. In one embodiment, the capacitor is a stacked container capacitor used in a dynamic random access memory circuit. The capacitor provides a capacitor that has high storage capacitance which provides an increased efficiency for a cell without an increase in the size of the cell.

38 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

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☐ 8. Document ID: US 6690040 B2

L6: Entry 8 of 20 File: USPT Feb 10, 2004

US-PAT-NO: 6690040
DOCUMENT-IDENTIFIER: US 6690040 B2

TITLE: Vertical replacement-gate junction field-effect transistor

DATE-ISSUED: February 10, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chaudhry; Samir	Orlando	FL		
Layman; Paul Arthur	Orlando	FL		
McMacken; John Russell	Orlando	FL		
Thomson; Ross	Clermont	FL		
Zhao; Jack Qingsheng	Orlando	FL		

US-CL-CURRENT: 257/135; 257/107, 257/133, 257/192, 257/204, 257/256, 257/260, 257/263, 257/272, 257/281, 257/288, 257/E21.447, 257/E21.629, 257/E27.06, 257/E27.069, 257/E29.313

ABSTRACT:

A vertical JFET architecture. Generally, an integrated circuit structure includes a semiconductor area with a major surface formed along a plane and a first source/drain doped region formed in the surface. A second doped region forming a channel of different conductivity type than the first region is disposed over the first region. A third doped region is formed over the second doped region having an opposite conductivity type with respect to the second doped region, and forming a source/drain region. A gate is formed over the channel to form a vertical JFET.

21 Claims, 18 Drawing figures
Exemplary Claim Number: 8
Number of Drawing Sheets: 8

☐ 9. Document ID: US 6559488 B1

L6: Entry 9 of 20 File: USPT May 6, 2003

US-PAT-NO: 6559488
DOCUMENT-IDENTIFIER: US 6559488 B1

TITLE: Integrated photodetector

DATE-ISSUED: May 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Thomas; Danielle A.	Dallas	TX		
Thomas; Gilles E.	Dallas	TX		

US-CL-CURRENT: 257/257; 257/461, 257/E27.132

ABSTRACT:

A photodetector is integrated on a single semiconductor chip with bipolar transistors including a high speed poly-emitter vertical NPN transistor. The

photodetector includes a silicon nitride layer serving as an anti-reflective film. The silicon nitride layer and oxide layers on opposite sides thereof insulate edges of a polysilicon emitter from the underlying transistor regions, minimizing the parasitic capacitance between the NPN transistor's emitter and achieving a high frequency response.

9 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw D

☐ 10. Document ID: US 6180442 B1

L6: Entry 10 of 20 File: USPT Jan 30, 2001

US-PAT-NO: 6180442
DOCUMENT-IDENTIFIER: US 6180442 B1

TITLE: Bipolar transistor with an inhomogeneous emitter in a BICMOS integrated circuit method

DATE-ISSUED: January 30, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gris; Yvon	Tullins			FR

US-CL-CURRENT: 438/202; 257/E21.375, 257/E21.696, 438/309, 438/344, 438/345, 438/349, 438/350, 438/365, 438/367, 438/368 , 438/370, 438/375, 438/377, 438/378, 438/482, 438/491, 438/525, 438/530, 438/532, 438/545, 438/548, 438/558, 438/559, 438/564

ABSTRACT:

The present invention relates to a method for fabricating an integrated circuit including an NPN-type bipolar transistor, including the steps of defining a base-emitter location of the transistor with polysilicon spacers resting on a silicon nitride layer; overetching the silicon nitride under the spacers; filling the overetched layer with highly-doped N-type polysilicon; depositing an N-type doped polysilicon layer; and diffusing the doping contained in the third and fourth layers to form the emitter of the bipolar transistor.

38 Claims, 17 Drawing figures
Exemplary Claim Number: 19
Number of Drawing Sheets: 7

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw D

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EPITAXIAL	49634
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